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Question Paper Code : 25084

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Third Semester

Electrical and Electronics Engineering

EE 8351 — DIGITAL LOGIC CIRCUITS

(Common to : Electronics and Instrumentation Engineering/Instrumentation and Control Engineering)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the DTL based NAND gate.

2. Perform subtraction on the following unsigned binary numbers using the 2's-complement of the subtrahend (a) 11011 – 11001 (b) 110100 –10101

3. Mention the dependency of output in combinational circuits.

4. Draw the NAND gate circuit using NOT, AND & OR Gates.

5. Write the role of master clock generator in synchronous circuits.

6. Comment about a preset table counter & ripple counter.

7. Draw the block diagram of asynchronous sequential circuit.

8. Outline about PLA.

9. Draw the basic structure of MOS transistor.

10. List the languages that are combined together to get VHDL language.

PART B — (5 × 13 = 65 marks)

11. (a) Assume a 3-input AND gate with output F and a 3-input OR gate with G output. Show the signals of the outputs F and G as functions of the three inputs ABC. Use all 8 possible combinations of inputs ABC. (13)

Or

(b) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa. (13)

12. (a) Given the following Boolean function $F = A'C + A'B + AB'C + BC$. (13)

(i) Express it in sum of minterms.

(ii) Find the minimal sum of products expression.

Or

(b) Draw the logic diagram of a 2-to-4 line decoder using NOR gates only. Include an enable input. (13)

13. (a) Explain the operation, state diagram and characteristics of a T flip-flop and master-slave JK flip-flop. (13)

Or

(b) Describe the design procedure with neat diagram about 4 bit bidirectional shift register with parallel load. (13)

14. (a) Discuss the operation of SR Latch with NOR and NAND gates analysis. (13)

Or

(b) Illustrate about hazards in sequential circuits and the steps to avoid hazards in it. (13)

15. (a) Explain the structure and working principles of TTL based Totem-pole output configuration. (13)

Or

(b) Write a VHDL code to realize a half adder using behavioral modeling and structural modeling. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Design a sequential circuit with two D flip-flops A and B, and one input x. When $x = 0$, the state of the circuit remains the same. When $x = 1$, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats. (15)

Or

(b) Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. when the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. (15)